CLAIMS

What is claimed is:

I claim:

1. A method, comprising:

performing a first test on a memory to detect defective components in the memory;

determining defective components in the memory from a first repair signature;

performing a second test on the memory to detect defective components in the memory;

allocating redundant components to repair the memory, if applicable; and

generating a second repair signature that repairs defective components represented in the first repair signature as well as defective components detected during the second test.

2. The method of claim 1, further comprising if the second test does not detect any defective components, then no redundant components are allocated.

3. The method of claim 1, further comprising:

performing the second test on the memory and the generation of the second repair signature after the memory has been placed into operation.

4. The method of claim 1, further comprising:

decoding the first repair signature to determine defective components in the memory.

5. The method of claim 1, further comprising:

performing the first test of the memory and a first repair algorithm on the memory to generate the first repair signature; and

performing the second test of the memory and a second repair algorithm to generate the second repair signature, the second repair signature repairing defective components detected by the first test as well as defective components detected by the second test.

6. The method of claim 1, further comprising:

testing the memory to identify defects under a first environmental condition;

next, testing the memory to identify defects under a second environmental condition; and

generating the second repair signature to repair all of the defects detected in the first environmental condition as well as in the second environmental condition.

7. The method of claim 6, wherein the first environmental condition comprises nominal temperature, nominal operating voltage level, and nominal frequency.

8. The method of claim 6, wherein the second environmental condition comprises higher than nominal temperature, higher than nominal operating voltage level, and lower than nominal frequency.

9. The method of claim 1, further comprising:

testing the memory to identify defects with a first type of testing algorithm;

next, testing the memory to identify defects with a second type of testing algorithm; and

generating the second repair signature to repair the defects detected with the first type of testing algorithm and the second type of testing algorithm.

10. An apparatus, comprising:

one or more memories, each memory having one or more redundant components to repair one or more defects detected in the one or more memories; and

a storage device to store a first repair signature that contains data to allocate the one or more redundant components;

reconfiguration logic to receive the first repair signature, the reconfiguration logic to augment the first repair signature by generating a second repair signature.

11. The apparatus of claim 10, wherein the reconfiguration logic further comprises:

logic to determine defective components in the one or more memories from the first repair signature, the logic to initiate a test on the memory to identify defective components, and the logic to generate the second repair signature.

12. The apparatus of claim 10, wherein the logic comprises electronic circuits that follow the rules of Boolean Logic and software that contain patterns of instructions.

13. The apparatus of claim 10, further comprising:

a processor having built in self-test logic, built-in self-diagnosis logic, built in redundancy allocation logic, and the reconfiguration logic.

14. The apparatus of claim 10, further comprising:

a volatile memory to store the second repair signature upon powering up the processor, content from the second repair signature to load into corresponding scan chain registers located in the one or more memories.

15. The apparatus of claim 13, wherein the processor programs one or more fuses contained in a fuse box with the second repair signature data.

16. A machine-readable medium that stores instructions, which when executed by a machine, cause the machine to perform operations comprising:

determining defective components in a memory from a first repair signature;

next, performing a test on the memory to identify defective components;

allocating redundant components to repair the memory, if applicable; and

generating a second repair signature that includes defective components represented in the first repair signature.

17. The article of manufacture of claim 16, which causes the machine to perform the further operations comprising:

programming the repair information into one or more scan chain registers located in each memory without programming any non-volatile fuses.

18. The article of manufacture of claim 16, which causes the machine to perform the further operations comprising:

testing the memory to identify defects under a first environmental condition;

next, testing the memory to identify defects under a second environmental condition; and

generating the second repair signature to repair all of the defects detected in the first environmental condition as well as in the second environmental condition.

19. The article of manufacture of claim 16, which causes the machine to perform the further operations comprising:

performing a first test of the memory and a first repair algorithm on the memory to generate the first repair signature; and

performing a second test of the memory and a second repair algorithm to generate the second repair signature, the second repair signature repairing defective components detected by the first test as well as defective components detected by the second test.

20. A memory compiler, comprising:

a machine-readable medium that stores instructions, which when executed by a machine, causes the machine to generate the apparatus of claim 10.

21. An apparatus, comprising:

means for performing a first test on a memory to detect defective components in the memory;

means for determining defective components in the memory from a first repair signature;

means for performing a second test on the memory to detect defective components in the memory;

means for allocating redundant components to repair the memory, if applicable; and

means for generating a second repair signature that repairs defective components represented in the first repair signature as well as defective components detected during the second test.

22. The apparatus of claim 21, further comprising:

means for testing the memory to identify defects under a first environmental condition;

means for testing the memory to identify defects under a second environmental condition; and

means for generating the second repair signature to repair all of the defects detected in the first environmental condition as well as in the second environmental condition.

23. The apparatus of claim 21, further comprising:

means for testing the memory to identify defects with a first type of testing algorithm;

means for testing the memory to identify defects with a second type of testing algorithm; and

means for generating the second repair signature to repair alldefects detected with either the first type of testing algorithm or with the second type of testing algorithm.

24. An apparatus, comprising:

one or more memories, each memory having one or more redundant components to repair one or more defects detected in the one or more memories; and

a storage device to store a first repair signature that contains data to allocate the one or more redundant components;

logic to generate an augmented repair signature to repair all of the defects detected in a first test of a memory as well as in a second test of the memory

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